Amendments to the Drawings:

Attachment: 10 Sheets of Formal drawings for Figures 1-16

REMARKS/ARGUMENTS

Claims 1-23 and 25-29 are pending the present patent application. Claims 1, 11-15, 21, 25, 27 and 28 have been amended. No new matter has been added to the amended claims. Claim 24 has been canceled. Reconsideration of the claims is respectfully requested.

A request for continued examination (RCE) is being filed herewith.

Summary of the Interview

Applicant would like to thank the examiner for the interview conducted on February 17, 2005. During the interview, a proposed amendment to the claims was discussed with the examiner. The applicant's representative explained to the examiner that the event trace memory 40 shown in the Klapproth patent was distinguishable from the programmable logic portion recited in the claims of the present application. The applicant's representative also pointed out that Klapproth does not provide any suggestion to combine a programmable logic portion, an embedded logic portion with a processor, and two JTAG circuits all into one integrated circuit, as recited in claim 1.

Objections to the Drawings

The office action objected to the application because it lacks formal drawings. To address this rejection, formal drawings for the present application are being submitted herewith.

Rejections of Claims 1-29

The office action rejected claims 1-29 as being obvious in view of U.S. Patent 5,590,354 to Klapproth.

A. Klapproth Does Not Disclose or Suggest All of the Elements of the Claims

Applicant has amended the claims to clarify the scope of the invention in light of Klapproth. Claim 1, for example, has been amended to recite "a programmable logic portion comprising a plurality of programmable logic cells configurable to perform logic functions." This amendment is supported by the present application, for example, at page 7, lines 4-8.

The office action asserted that the "programmable logic portion" of claim 1 reads on the event trace memory 40 in Klapproth. However, event trace memory 40 is not described in

Klapproth as being more than a standard memory. Klapporth does not describe event trace memory 40 as being a programmable logic portion that has a plurality of logic cells configurable to perform logic functions, as recited in amended claim 1.

In addition, Klapproth does not disclose or suggest a programmable logic portion, an embedded logic portion with a processor, and two JTAG circuits all on one single integrated circuit as recited in claim 1. Specifically, JTAG interface 30 and memory 40 are not shown as being on the same integrated circuit as CPU 60. See Figure 1 of Klapproth and col. 3, lines 8-32.

Claim 1 has also been amended to recite "at least some of the second plurality of data registers in the second JTAG circuit are designed to perform functions that are not performed by the first plurality of data registers." Klapproth does not disclose or suggest that JTAG interface circuits 30 and 46 have data registers designed to perform different functions.

B. The Claims Are Not Obvious in Light of Klapproth

Claim 1 recites an integrated circuit (IC) having an embedded logic portion and a programmable logic portion. The embedded logic portion of the IC includes a processor. The IC also has a first JTAG circuit for performing testing and/or debugging functions, and a second JTAG circuit. The second JTAG circuit augments the functionality of the first JTAG circuit.

The functionality of an existing JTAG circuit is limited by the hardware configuration of the data registers. To add additional testing and debugging functions, additional data registers must be added to the hardware design of the JTAG circuit in advance.

An existing programmable logic IC typically has to be redesigned to accommodate additional testing and debugging functions for data stored in the programmable logic circuitry. Redesigning an existing programmable logic IC involves the risk that the redesigned circuit may contain bugs that are not present in the original design. Plus, it takes time and effort to debug a newly designed circuit.

The present invention provides a substantially less risky option. New testing and debugging functions are added to the chip by simply adding a second JTAG circuit to the IC containing a second set of data registers that perform additional functions. The second JTAG circuit augments the functionality of the first JTAG circuit, instead of replacing it.

Klapproth does not disclose or suggest combining a processor and programmable logic onto a single IC, nor how to efficiently provide additional testing and debugging functionality to such an IC without redesigning an existing PLD architecture. Therefore, Klapproth would not have motivated one of ordinary skill in the art to combine a programmable logic portion, a processor, and first and second JTAG circuits onto a single IC as recited in amended claim 1.

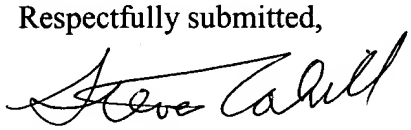
For at least these reasons, it is respectfully submitted that claim 1 is novel and nonobvious over the cited prior art references. The other claims are allowable for similar reasons.

CONCLUSION

In view of the foregoing, Applicants believe all claims now pending in this Application are in condition for allowance. The issuance of a formal Notice of Allowance at an early date is respectfully requested.

If the Examiner believes a telephone conference would expedite prosecution of this application, please telephone the undersigned at 650-326-2400.

Respectfully submitted,



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Attachments
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